CLAIMS

1. An address converter comprising:

an upper rank lookup table to sequentially output not more than m pieces of elements equivalent to a predetermined line of a m×n matrix having the number of the elements not less than the length of a predetermined address data row;

a lower rank lookup table to sequentially and repeatedly output n pieces of elements equivalent to said predetermined row of said m×n matrix not more than m times; and

an adder to add the output of said upper rank lookup table and the output of said lower rank lookup table and output said predetermined address data row.

2. An address converter according to claim 1,

wherein said address converter further comprises with a multiplier to multiply the output with m and input it in said adder instead of directly inputting the output of said lower rank lookup table in said adder.

3. An address converter according to claim 1 or 2,

wherein said adder adds the outputs of not less than three lookup tables.

4. An interleaver comprising:

said address converter according to claim 1,

a first register to hold a data row to be blended; and

a second register to register a data row of said first register in an order of the blending address data row on the basis of said blending address data row when an initial address data row is inputted in said address converter.

5. A deinterleaver comprising:

said address converter according to claim 1,

a second register to hold a data row to be blended; and

a first register to register a data row of said second register in an order of the initial address data row on the basis of the blending address data row when said initial address data row is inputted in said address converter.